Glossary of Acronyms Relevant to Electronics Manufacturing

ACI Automatic Component Insertion

ANSI American National Standards Institute

AOI Automated Optical Inspection. Test fixture method in which printed circuit boards are checked at bare-board, pre-or post-soldered stages of assembly by optical means.

ASIC Application Specific Integrated Circuit

ASM American Society of Metals

ASTE American Society Test Engineers

ASTM American Society for Testing and Materials

ASQC American Society Quality Control

ATE Automatic Test Equipment. Equipment designed to automatically analyze functional or static parameters in order to evaluate performance degradation. It may also be designed to perform fault isolation.

ATG Automatic Test Generation. Computer generation of a test program based solely on the circuit technology, requiring little or no manual programming effort.

BGA Ball Grid Array. A component whose terminations are on the bottom of the package, and are in the shape of solder balls and in a grid array pattern. This generally covers components that have them in a full array or in a partial array with “missing” balls in the center.

CAD Computer Aided Design. A computer based system to assist designers in the design, topological layout and drawing of an electronic component, assembly, or system.

CBGA/CCGA Ceramic Ball Grid Array/Ceramic Column Grid Array. A grid array packaged component that has ceramic as the substrate of the package, and may have either solder balls or solder columns for connections.

CFC Chlorinated Fluorocarbon.

CMA Circuit Mil Area. A unit of area equal to the area of a circle whose diameter is one mil (0.001”). Used chiefly in specifying cross-sectional areas of conductors.

CMOS Complementary Metal Oxide Semiconductor

CMT Chip Mount Technology. Any packaging or electronic assembly manufacturing technology, such as TOB, COB, or flip chip, that connects bare (unpackaged) IC chips to the substrate.

COB Chip-on-Board. A situation where the silicon IC chip is mounted directly to the electronic assembly substrate or PWB without an intermediate packaging step. Connections between the chip and the board are generally made with bond wired (also sometime called chip and wire), but the terminology is occasionally used for any chip connection technique such as flip chip (solderable bumps or tape automated bonding.

CSP Chip Scale Package. Active, multi-I/O package that is no larger than 125% of the size of the silicon IC.

CTE Coefficient of Thermal Expansion. See TCE

DFM Design for Manufacturability

DFT Design for Test

DIL Dual In-Line. Component shape with two parallel rows of connection leads.

DIP Dual In-Line Package. A popular through hole package with leads in rows on opposite sides of the package.

DRAM Dynamic RAM. Read-write memory that must be refreshed (read or written into) periodically to maintain the storage of information.

DUT Device Under Test. Component, PCB, or assembly subjected to a test. Also known as unit under test (UUT) and loaded board.

EIAJ Electronic Industries Association in Japan

ESD Electrostatic Discharge. A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.

ESS Environmental Stress Screening. Manufacturing stage in which all assemblies are subjected to abnormal stresses, with the aim of forcing all early failures to occur. Also known as reliability testing.

FCA Flip Chip Attach. The technique of attachment of an IC chip to a substrate using solderable bumps between the silicon chip and substrate.

FPT Fine Pitch Technology. The portion of surface mount technology that included components that typically have lead pitch, or center-to-center spacing, between 0.4mm and 0.8mm.

FP Flat Pack. A low profile IC package, which typically has gull wing type of leads on two or four sides.

FR-4 The most commonly used epoxy-fiberglass material standard for printed circuit boards. The “FR” refers to flame retardant.

HASL Hot Air Soldered Leveled. Hot air is used to blow off the excess after the PWB is dipped in solder. Typically used with the SMOBC process.

IC Integrated Circuit. A small, complete circuit made by vacuum deposition and other techniques, usually on a silicon chip, and mounted in a package.

IEEE Institute of Electrical and Electronics Engineers

ILB Inner Lead Bonding. Process of bonding termination, which leads to a tape automated bond integrated circuit's bumps.

IMAPS International Microelectronics and Packaging Society.

IMC Intermetallic Compound. Metallic compounds that form at the interfaces between different metals, such as copper-tin compounds that form at the interface of a solder joint and a copper lead. IMCs typically have significantly different properties, such as tensile strength.

IPC Institute for Interconnecting and Packaging Electronic Circuits

IR Infrared. Soldering process that uses infrared energy as the primary method of heating.

ISO International Standards Organization.

JEDEC Joint Electronic Devices Engineering Council, a part of the Electronic Industries Association (EIA) that publishes specifications and standards for electronic components.

KGB Known Good Board. A correctly operating PCB. It is used in learning or debugging a test program in development and for comparison testers where it serves as the standard unit by which other PCBs are compared.

KGD Known Good Die

LCCC Leadless Ceramic Chip Carrier (or CLCC for Ceramic Leadless Chip Carrier). A hermetically sealed ceramic package that has pads (castellations) around its sides for solder connection in a surface mounting application.

LDCC Leaded Ceramic Chip Carrier. A hermetically sealed ceramic package that has leads around its sided for solder connection in a surface mounting application. Typically, thee packages have over 28 leads.

LSI Large Scale Integration. Arrays of ICs on a single substrate that comprise 100 or more individual active circuit functions or gates.

MCM Multichip Module. A circuit comprised of two or more silicon devices bonded directly to a substrate by wire bond, TAB, of flip chip.

MELF Metal Electrode Face Bonding. A cylindrical leadless component with a round body and metals terminals on the ends.

MLB Mutli Layer Board. A PWB that has more than two conductor layers. The layers are interconnected by the plated-through holes.

MSD Moisture Sensitive Device.

MTBF Mean Time Between Failures. The arithmetic or statistical mean average time interval, usually in hours, that may be expected between failures of an operating unit. Results should be designated actual, predicted, or calculated.

MTTF Mean Time To Failure. Average time between failures.

MTTR Mean Time to Repair. A measure of how long it takes to access a failed system and identify, locate, and repair the fault.

OSP Organic Solder Preservative. Layers of organic coatings applied to entire boar surfaces to prevent oxidation and to retain solderability.

PBGA Plastic Ball Grid Array. A ball grid array component whose package substrate is made of plastic, most likely an FR-4 equivalent of epoxy-fiberglass, polyimide-arramid, or similar resin-fiber combinations.

PCA Printed Circuit Assembly. The generic term for a PCB after all electrical components have been attached. Also referred to as a printed wiring assembly (PWA).

PCB Printed Circuit Board. A part manufactured from a rigid base material upon which a completely processed printed circuit has been formed.

PGA Pad Grid Array. Similar to a pin grid array. An IC package that has solderable connections in a grid layout on the bottom of the package, and is soldered to the surface of the substrate (PWB) with butt solder joints.

PCMCIA Personal Computer Memory Card International Association. The organization that has developed the early standards for the various sizes of modules which were initially for memory expansion but are now used for many different electronic functions.

PLCC Plastic Leaded Chip Carrier. A plastic IC package for surface mounting applications that has leads, generally "J" leads, on all fours sides (sometimes given as PCC or PLDCC).

PPM Parts Per Million

PQFP Plastic Quad Flat Pack. An FP with leads on fours sides. Generally refers to a plastic quad flat package that is built to JEDC standards.

PTH Plated Through Hole. An interconnection from one side of a PWB (PCB) to another that is formed with the copper plating of the via (hole) sidewalls.

PWA Printed Wiring Assembly. The generic term for a PWB after all electrical components have been attached.

PWB Printed Wiring Board. The substrate, generally epoxy glass, used to provide component attachment lands and interconnections to form a functioning electronic circuit (also called a PCB or printed circuit board).

QFP Quad Flat Pack. A FP with leads on four sides. Generally refers to a plastic quad flat package that is built to EIJ standards.

QPL Qualified Products List. A listing of manufacturers qualified by test and performance verification to produce items listed in the MIL specs.

QSOP Quarter-Size Small Outline Package. An SO style IC package that has leads on a 25 mil pitch. The name derives from the fact that the package is approximately ½ the length and ½ the width of a standard SOIC, and thus a package of the same pin count occupies approximately ¼ the area on a PWB.

RAM Random Access Memory. A type of memory that offers access to storage locations within it by means of X and Y coordinates.

RCC Rectangular Chip Carrier. A chip carrier with unequal length and width dimensions.

ROM Read Only Memory. A random access storage in which the data pattern is unchangeable after manufacture.

SCC A chip carrier with a square body.

SIP Single-In-Line Package. An IC package or multi-component sub-assembly that has connections or leads in a single row on one side.

SIR Surface Insulation Resistance

SMA Surface Mount Assembly. An electronic assembly or module that is manufactured with surface mounted components and suing surface mount technology.

SME Society of Manufacturing Engineers

SMTA Surface Mount Technology Association

SMC (SMD) Surface mount components. Any electrical or mechanical component that can be attached to the surface of a substrate with solder.

SMOBC Solder Mask Over Bare Copper. A printed wiring board manufacturing technique whereby solder mask is applied over bare copper, exposed and developed, and then the board is dipped in molten solder to coat the exposed copper.

SMT Surface Mount Technology. The technology used to manufacture electronic assemblies using components that are soldered directly to the surface of the substrate or PWB.

SO Small Outline. A package resembling a flat pack with leads on only two sides.

SOIC Small Outline Integrated Circuit. A plastic IC package for surface mounting applications that has leads on two opposite sides.

SOJ A plastic IC package with “J” leads on two sides. It resembles a plastic DIP or an SOIC except for lead spacing and forming.

SOL/SOW Small Outline-Large/Small Outline Wide. SO generally refers to a package that is approximately 150 mils wide, while SOL/SOW refers to packages that are approximately 300 mils wide.

SOP VSOP/SSOP. Another designation for the small outline ICP packages, i.e. Small Outline Package (Very Small Outline Package, Shrink Small Outline Package)

SOT Small Outline Transistor. A plastic leaded package for diodes and transistors used in surface mounting applications.

SPC Statistical Process Control. The use of statistical techniques to analyze a process or its output to determine any variation from a benchmark and to take appropriate action to restore statistical control, if required.

SSOIC Shrink Small Outline IC. An SO style IC package that has leads on a 25 mil pitch.

TAB Tape Automated Bonding. An IC interconnection process that uses organic tape to support pre-formed leads during bonding to the chip (inner lead bonding-ILB) and connection to the substrate (outer lead bonding-OLB). The IC chip is usually bare during the interconnecting processes.

TBGA Tape Ball Grid Array. A ball grid array component package that uses TAB techniques to make the connections between the IC chip and the solder balls. This results in a solder ball grid array that is only around the periphery, and leaves compliant connections between the IC and the solder balls for better TCE reliability.

TCE (CTE) Thermal Coefficient of Expansion (Coefficient of Thermal Expansion). The rate of expansion (ppm/C) of a material when its temperature is increased.

VFP Very Fine Pitch. The center-to-center lead distance of surface mount packages that are between 0.012 inch and 0.020 inch.

VLSI Very Large Scale Integration

VSP Vapor Phase Soldering. Soldering accomplished by using heat generated by the condensing of a vapor ion a cooler assembly. VSP is achieved with SMT by using a high temperature, approximately 215 degrees C, special prefluorinated fluid.

VSOIC Very Small Outline IC. An SO style IC package that has leads with a pitch of 30 mils or less.

Sources Used:

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"Surface Mount Technology: Principles and Practice", Ray Prasad, 1997.
"Surface Mount Technology Terms and Concepts", Phil Zarrow and Debra Kopp, ITM, 1997.